



## **A NEW ERA FOR DOLPHIN INTEGRATION'S EMBEDDED MEMORIES**

Grenoble, July 14, 2008. Dolphin Integration is announcing a blockbuster sRAM Trio for embedding in circuits at 130 nm in G process and at 90 nm in LP process.

The Low-Power Library Provider extends their offering with URANUS sRAM in three variants at once: LCL (Low in Consumption and Leakage) already celebrated in users' designs, BCD (Best in Consumption and Density) up to 20 % denser for a slight increase in consumption, and LLA (Low Leakage Acute) with a mere 5 % extra area for consuming 30 times less than free libraries.

Not surprisingly this new generation of URANUS also exploits the flexibility granted by the recently disclosed SESAME patent, which gives its unique strength to the standard cell library.

Their continued presence amidst the giants of microelectronics over the last quarter of a century provides the Dolphin team with a unique insight into the truisms of this industry. While some of the big actors threatened by microelectronics deverticalization are still resisting it, the foundries, true winners in this irreversible change, are now attempting to reverticalize on their own power base. Freedom of innovation in design is the cornerstone. Any monopolistic temptation, such as it can be seen simultaneously in the EDA-CAD domain, not only is a sign of weakness, but generates its own backlash in an industry which must preserve its dynamism. Both attempts, from the Silicon foundries and from the EDA providers, are causes of concern for the future of the Fabless actors, lest second sourcing or even freedom of choice for the best supplier, would be severely hampered by a combination of business models and technical incompatibilities.

With their charter to enable integration mixed signal Systems-on-Chips, the Dolphin designers have managed a memory development program enabling to optimize separately bit-cells amenable to foundry-captive Design-Rule Pushing, and Memory Structures facilitating technological retargeting. This effort is of growing importance because the number of technological variants at each process node is multiplying.

*"This is not a time for procrastinating to address the need for a rich diversity in memory performances, remarks Agnès Venet, Manager of the Silicon IP development Lines at*

Dolphin Integration, *while the spread of active technological nodes renders the feasibility of smooth retargeting, from process to process, just the more crucial*".

More process options shall follow suit for URANUS at 65 nm to begin with and at half nodes. Consistently launching three well-differentiated variants at once of the same Memory Structure addresses the challenge of safely proving the worth of each design variant on Silicon: it is simplified by their familiness.

For the Board of Directors, the Executive Chairman.

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## About Dolphin

Dolphin Integration is up to their charter as the most adaptive creator in Microelectronics to "enable mixed signal Systems-on-Chip", with a quality management stimulating reactivity for innovation.

Their current mission is to supply worldwide customers with fault-free, high-yield and reliable sets of CMOS Virtual Components, resilient to noise and drastic for low power-consumption, together with engineering assistance and product evolutions customized to their needs.

DOLPHIN Integration SA with social Capital of 1,295,120 € - [www.dolphin.fr](http://www.dolphin.fr)  
ISIN: FR0004022754/ ALDOL – Bloomberg: ALDOL FP – Reuters: ALDOL.PA  
ICB 9576. Semiconductors.

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