

## **DOLPHIN INTEGRATION**

**SLED**

**New Features**

**October 12, 2018**

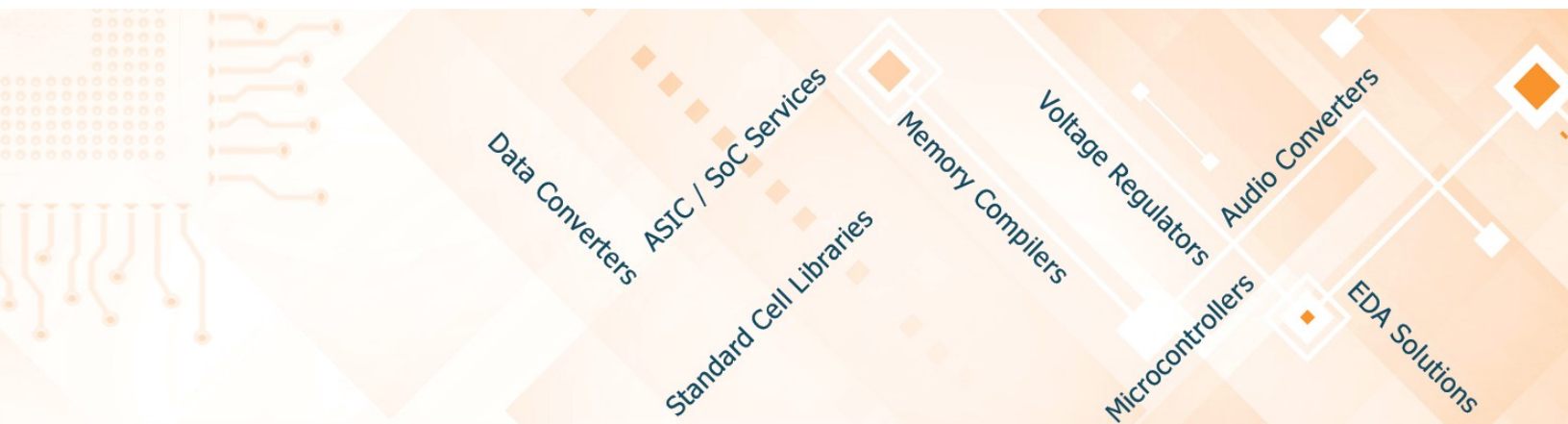
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## THANKS

As always for new releases, we would like to thank those customers who take the time to report problems and/or to suggest improvements (please remember that the best way to do so is by sending an email to [medal@dolphin-integration.com](mailto:medal@dolphin-integration.com) or [support@dolphin-integration.com](mailto:support@dolphin-integration.com) with an accurate description of your problem or suggestion, together with the relevant files if any). As you will see in the new features, we do our best to take remarks into account. And even if your suggestion does not appear this time, don't think it was lost or disregarded. Simply, it means that its implementation could not fit into the development plan for this particular release, but be assured that we will try to take it into account in a future release.

## WEB SITE

Our web site <http://www.dolphin-integration.com> is a source of information on our EDA solutions. Aside from evaluation kits for our products, a number of application notes, courses or upgrades are available for download.

## SLED

SLED is a hierarchical schematic entry solution of the third generation which delivers the long awaited dual capability for Graphic Entry and Scriptability at once. It blends efficiently the feasibility of linking components and of writing scripts for configuring a netlist hierarchically. Interoperability with other schematic entry tools is ensured for capitalizing on legacy designs and cooperative work, and interoperability in the Design Chains is ensured through standard design exchange formats and scriptability for customization by CAD managers.

## PSL

Relevant options of SMASH include native support for simulation of PSL<sup>1</sup> properties, both assertions and coverage, with very low time and memory overhead.

The integration of PSL is complete with source code syntax coloring, association of verification units with Verilog or VHDL models or instances, logging of PSL assertion violations, reporting of PSL sequence coverage results, and breaking into the source level debugger for investigation of design defects.

## Assertion-Based Verification

The SLED SDG<sup>2</sup> option enables conversion of PSL assertions into synthesizable RTL models. This makes it possible for the designer to automatically integrate PSL verification units into a Design Under Test in an FPGA for emulation or in a testchip. Embedding hardware verification units in prototypes increases verification speed by several orders of magnitude.

Automated generation of synthesizable models from PSL assertions can also be used as an efficient alternative to writing safety related parts of a design directly in RTL. These hardware verification units are integrated for embedded monitoring.

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<sup>1</sup>Property Specification Language

<sup>2</sup>Synthesizable Detector Generator

## **SUPPORTED PLATFORMS**

### **Microsoft Windows**

SLED is designed to run on Microsoft Windows Vista / 7 / 8 / 10 on x86\_64 platforms.

### **Linux on Intel x64 platform**

SLED is designed to run under X-Window on RedHat Enterprise Linux 6 (RHEL6) and supports compatible Linux distributions on x86\_64 platforms.

## CREDITS & COPYRIGHTS

### Qt : A C++ framework for cross-platform programming

<http://qt.digia.com>

Qt Development Frameworks creates application development platforms for desktop and mobile device innovation.

Qt Development Frameworks igia Oyj, Valimotie 21, 00380 Helsinki Finland +358 10 313 3000  
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### Scintilla Source Code Editor Component

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### LIBJSON Component

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## SLED

### SLED

#### Enhancements

- Implemented the ability to display Back annotation results grouped according to different severity (DDIsa13078 - SLED 3.2.0)
- Implemented the detection parameter definitions which are not defined on cells (DDIsa13141 - SLED 3.2.0)
- Implemented an ability to send user feedback and support from the interface (DDIsa13150 - SLED 3.2.0)
- Implemented the management of the –etc-dir and –user-dir parameters in the SLED command line argument to define alternative application and user directories (DDIsa13156 - SLED 3.2.0)

#### Bug fixing

- Corrected the ability to delete cells by the "Delete" menu item (DDIsa12600 - SLED 3.2.0)
- Corrected the display of a warning message in the Output window when no occurrence is found after using the Quick Search tool (DDIsa12707 - SLED 3.2.0)
- Corrected the display of backannotation bubbles when schematic has several sheets (DDIsa12965 - SLED 3.2.0)
- Corrected the Scan for Changes behavior on cell names that contain a space character (DDIsa12986 - SLED 3.2.0)
- Corrected the un-expected activation of the Line Numbers command when the command Selection Marging is activated in the text editor (DDIsa12989 - SLED 3.2.0)
- Corrected the focus on the search field after a failed search (DDIsa12990 - SLED 3.2.0)
- Corrected the un-expected position changing of backannotation bubble when adding a graphic object in the sheet (DDIsa12992 - SLED 3.2.0)
- Corrected the multi-pins handling from the Pin Number Tool (DDIsa12995 - SLED 3.2.0)
- Removed the possibility to set a null angle on an arc (DDIsa13004 - SLED 3.2.0)
- Corrected the renaming of document in the Project manager (DDIsa13005 - SLED 3.2.0)
- Corrected an application crash after using the Go To Instance command in the Hierarchy browser (DDIsa13009 - SLED 3.2.0)
- Corrected an application crash when using instances filter in the Hierarchy browser on a large design (DDIsa13010 - SLED 3.2.0)
- Corrected the hierarchical name provided in the Query panel when the net is a bundle (DDIsa13044 - SLED 3.2.0)



- Corrected the enable status of the Parse command after deleting a hierarchical object (Document, CellView, Cell) which has been copied in the application clipboard. (DDIsa13121 - SLED 3.2.0)
- Corrected the increase of the netlisting process delay when several netlists are generated sequentially for the same schematic (DDIsa13128 - SLED 3.2.0)
- Corrected the result of the find process when searching instances with parameter criteria (Name and/or Value) (DDIsa13133 - SLED 3.2.0)
- Improved the documentation concerning the the Spice.InstanceParameters in the SLED User Manual documentation (DDIsa13175 - SLED 3.2.0)
- Displayed error message when the view renaming process failed (DDIsa13195 - SLED 3.2.1)
- Corrected the handling of net label offset from the Property Editor (DDIsa13196 - SLED 3.2.1)

## SLED API

### Enhancements

- Implemented the SLED API function SLED\_HierObjAddDoc for adding document in hierarchical objects (Design, Library and Cell) (DDIsa13183, DDIsa13036 - SLED 3.2.0)

### Bug fixing

- Corrected the SLED API function SLED\_DesignSave which removed the content of model files when the inIsSaveForce argument was set to true (DDIsa12985 - SLED 3.2.0)