

## **DOLPHIN INTEGRATION**

**SLED 3.3.0**

**New Features**

**December 17, 2018**

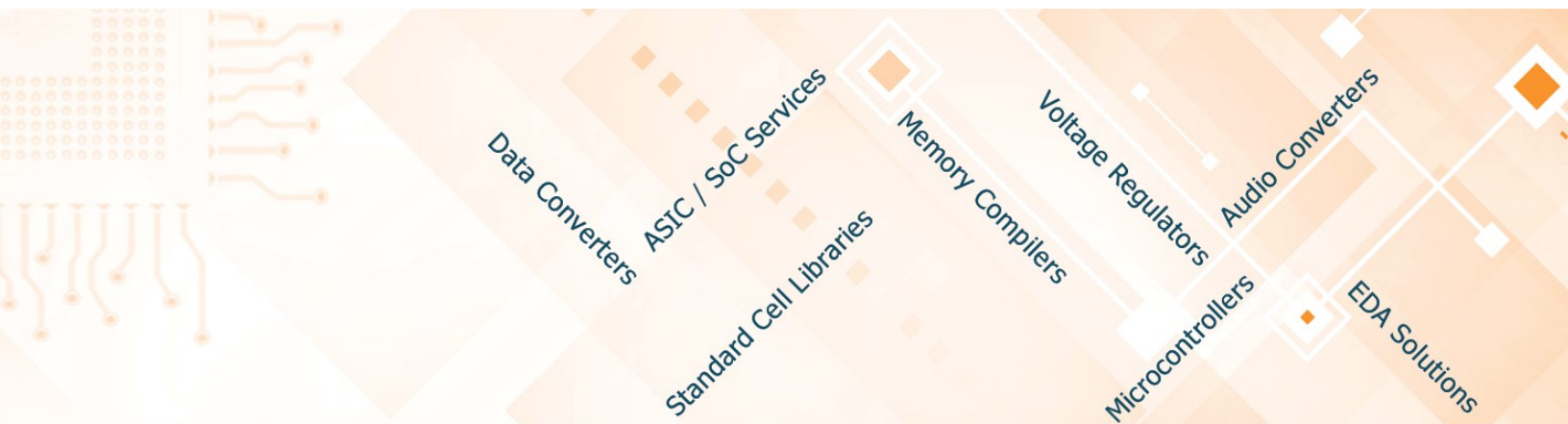
**Dolphin Integration**

39 Avenue du Granier - BP 65 - Inovallee - 38242-MEYLAN - FRANCE

Phone : + 33 4 76 41 10 96 - Fax : + 33 4 76 90 29 65

[www.dolphin-integration.com](http://www.dolphin-integration.com)

[contact@dolphin.fr](mailto:contact@dolphin.fr)



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## THANKS

As always for new releases, we would like to thank those customers who take the time to report problems and/or to suggest improvements (please remember that the best way to do so is by sending an email to [medal@dolphin-integration.com](mailto:medal@dolphin-integration.com) or [support@dolphin-integration.com](mailto:support@dolphin-integration.com) with an accurate description of your problem or suggestion, together with the relevant files if any). As you will see in the new features, we do our best to take remarks into account. And even if your suggestion does not appear this time, don't think it was lost or disregarded. Simply, it means that its implementation could not fit into the development plan for this particular release, but be assured that we will try to take it into account in a future release.

## WEB SITE

Our web site <http://www.dolphin-integration.com> is a source of information on our EDA solutions. Aside from evaluation kits for our products, a number of application notes, courses or upgrades are available for download.

## SLED

SLED is a hierarchical schematic entry solution of the third generation which delivers the long awaited dual capability for Graphic Entry and Scriptability at once. It blends efficiently the feasibility of linking components and of writing scripts for configuring a netlist hierarchically. Interoperability with other schematic entry tools is ensured for capitalizing on legacy designs and cooperative work, and interoperability in the Design Chains is ensured through standard design exchange formats and scriptability for customization by CAD managers.

## PSL

Relevant options of SMASH include native support for simulation of PSL<sup>1</sup> properties, both assertions and coverage, with very low time and memory overhead.

The integration of PSL is complete with source code syntax coloring, association of verification units with Verilog or VHDL models or instances, logging of PSL assertion violations, reporting of PSL sequence coverage results, and breaking into the source level debugger for investigation of design defects.

## Assertion-Based Verification

The SLED SDG<sup>2</sup> option enables conversion of PSL assertions into synthesizable RTL models. This makes it possible for the designer to automatically integrate PSL verification units into a Design Under Test in an FPGA for emulation or in a testchip. Embedding hardware verification units in prototypes increases verification speed by several orders of magnitude.

Automated generation of synthesizable models from PSL assertions can also be used as an efficient alternative to writing safety related parts of a design directly in RTL. These hardware verification units are integrated for embedded monitoring.

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<sup>1</sup>Property Specification Language

<sup>2</sup>Synthesizable Detector Generator

## SUPPORTED PLATFORMS

### Microsoft Windows

SLED is designed to run on Microsoft Windows Vista / 7 / 8 / 10 on x86\_64 platforms.

### Linux on Intel x64 platform

SLED is designed to run under X-Window on RedHat Enterprise Linux 6 (RHEL6) and supports compatible Linux distributions on x86\_64 platforms.

## CREDITS & COPYRIGHTS

### Qt : A C++ framework for cross-platform programming

<http://qt.digia.com>

Qt Development Frameworks creates application development platforms for desktop and mobile device innovation.

Qt Development Frameworks igia Oyj, Valimotie 21, 00380 Helsinki Finland +358 10 313 3000  
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### Scintilla Source Code Editor Component

License for Scintilla and SciTE

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### LIBJSON Component

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## SLED

### SLED

#### Enhancements

- Parameter definition is now allowed only on cell (DDIsa13311 - SLED 3.3.0)
- Implemented the ability to display only the parameters that are relevant to the current design configuration (DDIsa13348 - SLED 3.3.0)
- Implemented the ability to set a background color and pattern on symbol instance (DDIsa13355 - SLED 3.3.0)
- Improved the SLASH device library to take into account units and descriptions of the parameters, as well as colorization of instances (DDIsa13378 - SLED 3.3.0)

#### Bug fixing

- Corrected the handling of the selection by the Duplicate Tool (DDIsa13187 - SLED 3.3.0)
- Corrected the text case handling in the hierarchical name information of the Project Manager items (DDIsa13194 - SLED 3.3.0)
- Corrected the application crash when creating a new cell with a name that contains the '%' character (DDIsa13271 - SLED 3.3.0)
- Fixed the display of modified views which are multiple displayed (DDIsa13352 - SLED 3.3.0)
- Corrected the backannotation results display when a schematic view doesn't have the same name as its cell (DDIsa13353 - SLED 3.3.0)
- Fixed the modification of the background color of power port (DDIsa13371 - SLED 3.3.0)
- Set the Read-Only status for the Description widget, when the description text has the HTML format (DDIsa13375 - SLED 3.3.0)

## SLED API

#### Enhancements

- Implemented custom API functions to ease the objects retrieval (DDIsa12664, DDIsa12663 - SLED 3.3.0)
- Implemented the SLED API function SLED\_AddDisciplineCompatibilityRule for adding a discipline compatibility rule (DDIsa13281 - SLED 3.3.0)
- Implemented SLED API function SLED\_DesignImportConfiguration for importing a configuration file into the design (DDIsa13324 - SLED 3.3.0)



**Bug fixing**

- Corrected the management of Url parameter in the SLED Hooks (DDIsa13342 - SLED 3.3.0)

**SLED DRC****Enhancements**

- Completed the 'Incorrect object name' rule for checking that no instances have the same name as a net name (DDIsa09524 - SLED 3.3.0)
- Implemented means to add new erc rules defined in tcl script (DDIsa13252 - SLED 3.3.0)
- Implemented means to define erc rules for cell with the SLED API (DDIsa13267 - SLED 3.3.0)
- Implemented the Erc rule 'Hierarchical parameter not defined' which checks that hierarchical parameter used in instance parameter value is defined at the upper level (DDIsa13285 - SLED 3.3.0)

**Bug fixing**

- Corrected application crash when an ERC is performed on schematic which contains instance with hierarchical parameter (DDIsa13253 - SLED 3.3.0)
- Corrected the result of a heriarchical which can be not consistent (DDIsa13262 - SLED 3.3.0)
- Corrected the selection of net when a rule violation net link is activated (DDIsa13265 - SLED 3.3.0)
- Corrected the un-expected violation of the 'Net not driven' rule when a net is connected to ignored instance pin (DDIsa13268 - SLED 3.3.0)
- Corrected the behavioral of the 'Net not driven' rule when not has no wire (DDIsa13269 - SLED 3.3.0)
- Renamed the ERC rule "Hidden nets" to "Hidden propagated instance pins" and fixed the link associated with the violation item (DDIsa13274 - SLED 3.3.0)
- Corrected the behavior of links associated with nets which violate the 'Implicit connection in schematic' rule (DDIsa13275 - SLED 3.3.0)
- Modified the list of items provided by the violation of the rule 'Implicit connection in sheet' (DDIsa13276 - SLED 3.3.0)
- Corrected the wrong violation of the rule 'Duplicated pin number' when the symbol to check has several pins with the same name (DDIsa13277 - SLED 3.3.0)
- Renamed the Erc rule 'Duplicated pin name' to 'Pin name conflict' (DDIsa13278 - SLED 3.3.0)
- Corrected the behavior of links associated to instances which violate the rule 'Empty instance property value' (DDIsa13280 - SLED 3.3.0)
- Corrected the behavioral of 'Unconnected input pin' rule when it is applied on instance which has several propagated pins (DDIsa13286 - SLED 3.3.0)
- Corrected the behavioral of 'Unconnected Input/Output/Bidirectional port' matrix rules when they are applied on schematic with instance(s) (DDIsa13304 - SLED 3.3.0)