A versatile Control Network of power domains in a low power SoC

1. INTRODUCTION

With the development of more and more power-consuming mobile applications, the battery lifetime has become the biggest challenge of a low-power System-on-Chip (SoC).

Success in designing a low-power SoC requires successive attention to five intertwined networks:

- the exchange network between functional blocks through data busses,
- the clock distribution network, possibly enabling clock gating and frequency scaling,
- the voltage regulation network, possibly enabling Dual Voltage and Frequency Stepping (DVFS),
- the control network of power islands, managing changes of power modes implying transitions of clock frequencies and voltage regulator states,
- the application network which spans over the PCB.

Developing and verifying a control network in a low-power SoC is a challenging task, especially managing the different states of regulators and modes of power domains.

This article first describes state-of-the-art approaches to addressing this issue, and then delves into the solution promoted by Dolphin Integration to go further, thanks to the easy and secure Maestro™ solution to manage SoC power mode transitions.

2. CONTROL NETWORK DESIGN SOLUTIONS

When using advanced design techniques to reduce power consumption through the introduction of power domains, SoC states and power modes are managed by designing a Power Management Unit (PMU) or an Activity Control Unit (ACU) to supply and control the power domains. These are fundamentally SoC specific constructs, which can be designed in two distinct ways:

- Using a monolithic approach, SoC integrators design a centralized scheme. The design and verification is often long and complex due to the lack of a hierarchically structured and modular approach for interconnections, placement and control, resulting in a low rate of re-use of elementary components, be they oscillators, voltage regulators or control modules.

- Using a modular approach, SoC Integrators can design a network of interconnected elements in order to:
    - Enable local modifications without cross-impacting the rest of the supply network or of the control network, when facing the need for architectural upgrades. Each modification thus impacts one regulator or one hardware module of the control network, not the complete hardware controller,
    - Reuse modules several times in the design to control similar operations,
    - Ease the top-level verification thanks to a determined number of elements with predefined functionalities.

Maestro™ is a modular solution dedicated to easing the control of frequency, voltage and mode transitions for the power domains of low-power SoCs. Due to its focus on power mode management and scalability, Maestro™ is the perfect solution for a wide range of low-power SoC complexities.

Other modular solutions are available on the market for the design of Networks-on-Chip (NoC), which are often mingled with the two previous solutions. NoC solutions are dedicated to data management in complex sub-systems where data is difficult to manage, as in the context of multi- or many-processor sub-systems. A NoC can manage data packet transmission between blocks by taking into account the state of each block.

The Maestro™ solution relies on different rules:

- The subsidiarity principle with modular design thanks to generic and customizable modules, which structure the design of the ACU/PMU. Each module is dedicated to a type of island or resource in order to functionally manage its mode transitions, be it a power domain or island, voltage regulator, clock generator, etc.
- Smart combination of one soft (C/C++) and six synthesizable RTL modules for a good compromise between flexibility and time-to-market.
- Automatic management of conflicts between resources by Maestro™ modules.
- A dedicated control bus independent from data busses, thus authorizing the construction of the power island architecture over the functional block architecture. It enables switching-off higher speed data busses, the control bus being always-on but at low-frequency.

- Consistency with the construction of power domains per the UPF for turning them into islands endowed with the patented "Transition Ramp Cells" of Dolphin Integration's Island Construct Kit to optimize the in-rush current of each domain.
- The simplicity of the communication protocol.

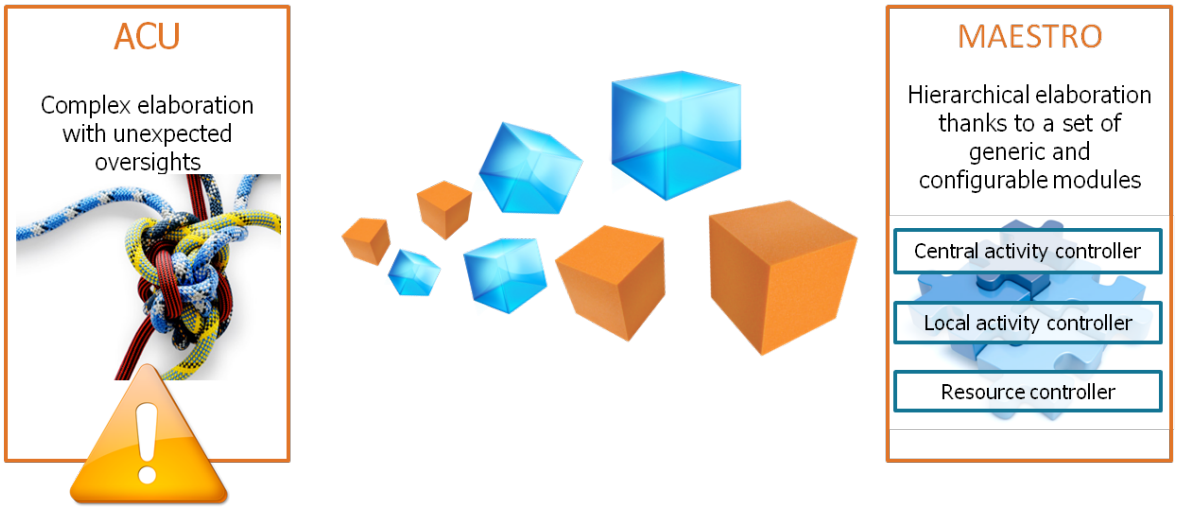

Figure 1: ACU vs. Maestro™

3. MAESTRO™ SYNCHRONOUS FABRIC

Maestro™ is a synchronous fabric dedicated to the control of the modes of power domains. The major innovation consists in separating two busses for linking any peripheral block or island: the standard peripheral bus (SFR, AHB…) for data transmissions and a dedicated control bus (part of the Maestro™ fabric) for the control of the modes of power domains. Maestro™ provides a new standard for introducing reusable control components which interact with SoC power domains and associated resources: voltage regulator, clock generator, etc. It enables dodging the most error-prone phases of either a top-down or a bottom-up SoC integration process. It is based on a set of generic and customizable components which can be assembled to manage the mode transitions of a SoC.

The main components of a Maestro™ network are the following:

- **Mode Switching Program (MSP):** brain of a Maestro™ network. It knows the list of modes of the SoC along with the state of each island for each mode, and manages the sequences to switch from one SoC mode to another. For SoC containing a processor, the SoC power state table and the mode transition sequences are implemented as software executed by the processor.

- **CentralActivity Controller:** component which manages the start-up sequence (inital boot) of the SoC as well as the power on and power off sequences of the MSP to enter into and wake-up from sleep modes. The Central Activity Controller is also a bridge between the system bus and the Dedicated Control Bus.

- **Local Activity Controller:** local interface for a power domain which receives the mode change requests from the Dedicated Control Bus, knows the list of modes of the connected power domain with the corresponding state of its resources (voltage regulator, clock generator or divider, etc.). It manages the sequence of transitions of the island and associated resources corresponding to the mode changes requested by the Central Activity Controller.

- **Dedicated Control Bus:** standardized control bus which connects the different components of Maestro™. All mode change requests (power state, frequency and voltage level) are transmitted through this dedicated control bus.

- **Resource Controller:** component which manages the state of its associated resources (voltage regulator, clock generator or supply reference). It arbitrates resquests from different Local Activity Controllers and sets its resources in the most approriate mode. To ease the control of resources and the definition the power modes of the SoC, a set of parameters are defined. The parameter settings are configurable for every resource.

- **SmartVision:** Interactive Development Environment of the third generation to facilitate debug of software by supporting the hardware of a "Built-In Realtime Debugger" (BIRD) amidst the graphic representation of the overall synopsis as on Figure 2.

4. HOW DOES MAESTRO™ WORK?

Based on such a synopsis, possible interactions between the different components can be:

- The Mode Switching Program receives a request to change the SoC mode. It activates a sequence of island mode changes (below change mode of power domain B)

- The Mode Switching Program sends a mode change request through the peripheral bus to reduce the consumption of the power domain B.
- The Central Activity Controller sends the request over the Dedicated Control Bus.
- The target Local Activity Controller decodes the request, sends the request to the associated Resource Controller and changes the configuration of power domain B.
- The Resource Controller selects the most appropriate mode for its associated resources regarding the status of all its Local Activity Controllers.
- The Mode Switching Program is informed of the status of the power domain B.

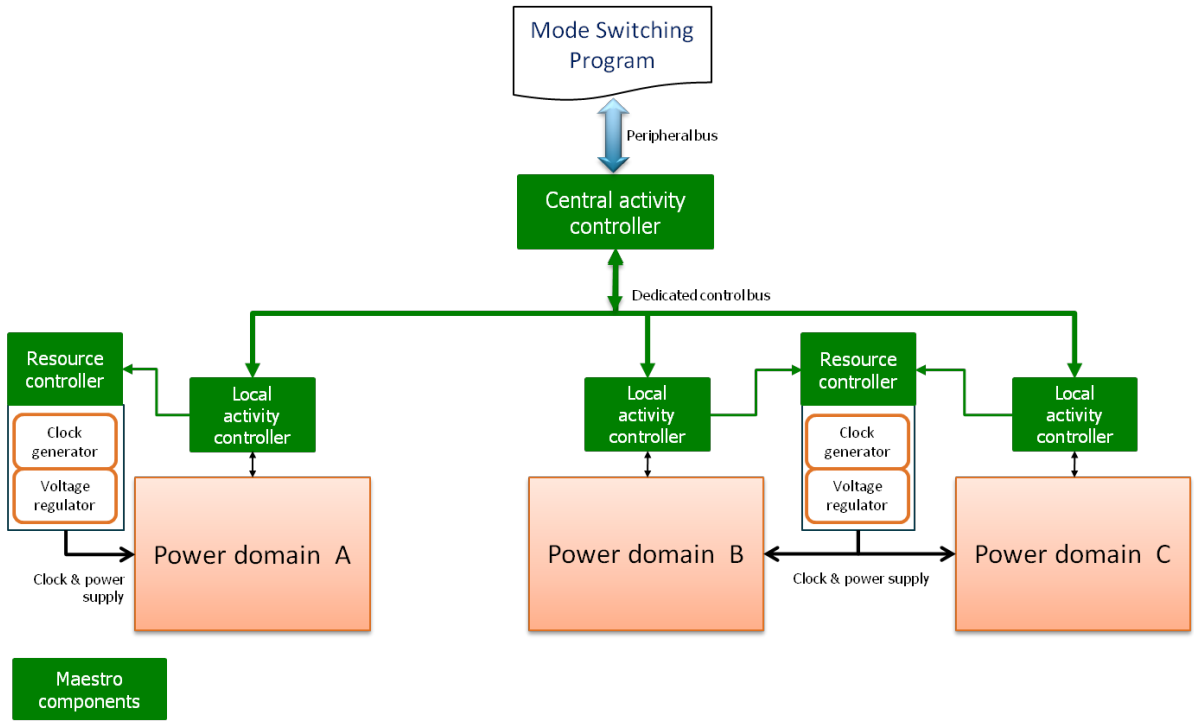

Figure 2: Example of Maestro™ insertion into a SoC

5. A READY TO USE SOLUTION

Maestro™ is a patent pending solution ready to be used and delivered to any customer. It is based on synthesizable RTL blocks plus guidelines for MSP development and top-level assembly. It has been successfully implemented in a low-power Demonstration testchip at 55nm, with six power domains and four embedded regulators, controlled by Maestro™.

It is worth noticing that all Maestro™ modules belong to the Always-On domain, within which the power islands are embedded: it enables either Maestro™ laid-out as scattered modules, or gathered as a compact ACU.

This Demonstration testchip represents a typical MCU application connected to several internal and external memories. A Whisper trigger™ for "Voice Activity Detection" (VAD) is in the always-on power domain, waiting for an external signal to wake up the system.

More information on Maestro on Dolphin Integration website.

About the author

Gauthier Reveret has joined Dolphin Integration in 2012 as digital design engineer in microcontrollers team. He is now involved in low power SoC architecture design.
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About Dolphin Integration

Dolphin Integration contributes to "enabling low-power Systems-on-Chip" for worldwide customers - up to the major actors of the semiconductor industry - with high-density Silicon IP components best at low-power consumption.
The "Foundation IP" of this offering involves innovative libraries of standard cells, register files and memory generators. The "Fabric IP" of voltage regulators, Power Island Construction Kits and their control network MAESTRO enable a flexible assembly with their loads. They especially star the "Feature IP": from high-resolution converters for audio and measurement applications to power-optimized 8 or 16 and 32 bit micro-controllers.

Over 30 years of experience in the integration of silicon IP components, providing services for ASIC/SoC design and fabrication with its own EDA solutions, make Dolphin Integration a genuine one-stop shop addressing all customers' needs for specific requests.
It is not just one more supplier of Technology, but the provider of the DOLPHIN INTEGRATION know-how!
The company strives to incessantly innovate for its customers' success, which has led to two strong differentiators:

- state-of-the-art "panoplies of Semiconductor IP components" for high-performance applications securing the most competitive SoC architectural solutions,

- a team of Integration and Application Engineers supporting each user's need for optimal application schematics, demonstrated through EDA solutions enabling early performance assessments.

Its social responsibility has been from the start focused on the design of integrated circuits with low-power consumption, placing the company in the best position to now contribute to new applications for general power savings through the emergence of the Internet of Things.