

CHALLENGE - OPTIMIZATION

Active battery-powered RFID applications are strict on power requirements. With lifetime ratings of many years without battery replacement, SoCs and the involved regulators must be extremely efficient.

During normal operation, when the tag is transmitting its ID, the load current is generally between a few milliamps to hundreds of milliamps depending on the application and standards.

During standby, power is limited to maintaining the wakeup circuitry. Most of the tag life is spent in this mode, where currents must be kept below a few microamps.

Dolphin Integration's low-quiescent hysteresis comparators are designed to operate as a pair and their are ideal for these applications.

qCMPH-RR-[2.0-3.63]-[1.2-1.98].02 is a fast hysteresis comparator, designed to extract data from the RF waveform in normal mode operation. Although it consumes a bit more than its wakeup counterpart, it only draws a current of 9 μA to save on battery energy even in the most power-critical applications.

qCMPH-LP-[2.0-3.63]-[1.2-1.98].02 is designed to detect the waveform amplitude level, in order to wake up the system when the tag is brought close to a checkpoint. This comparator only draws a current of 600 nA, thereby maximizing battery life.

KEY BENEFITS

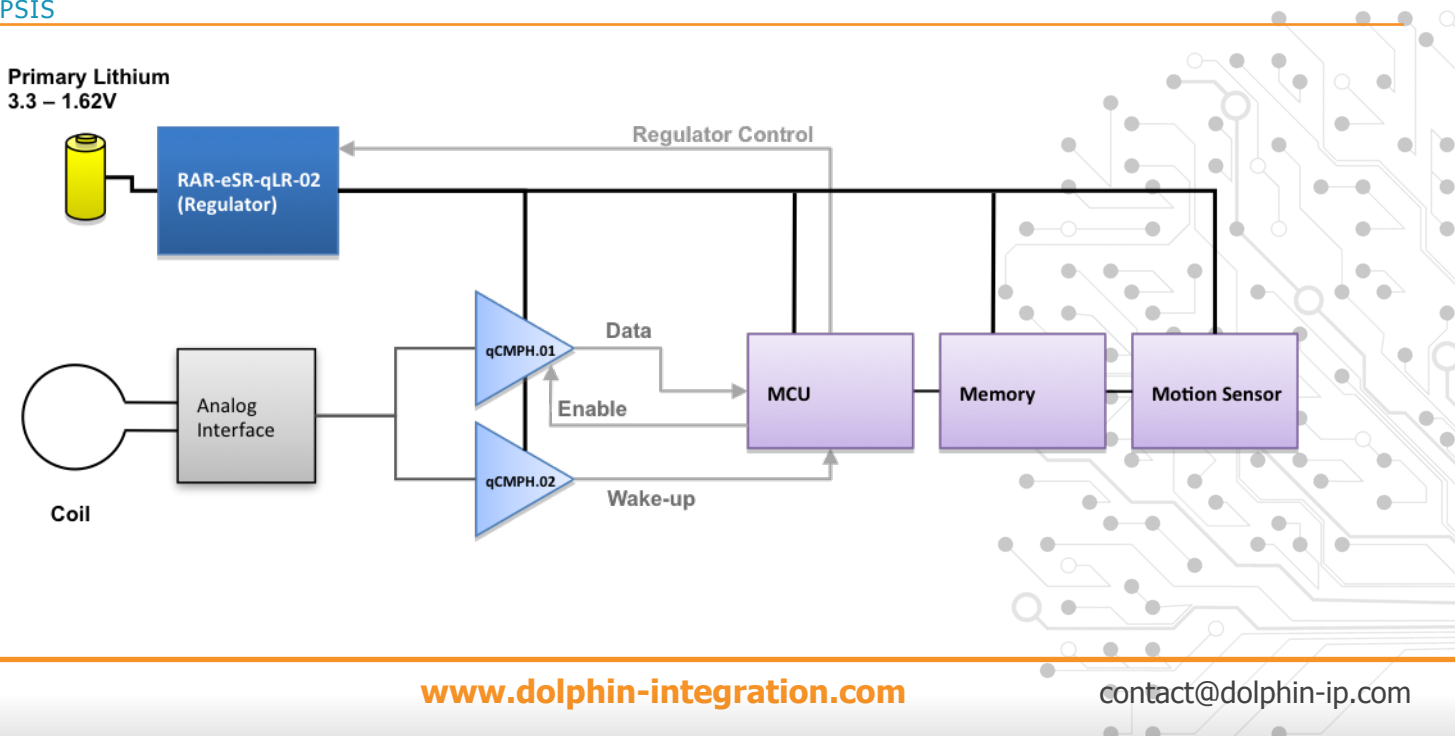
- **qCMPH-RR-[2.0-3.63]-[1.2-1.98].02**

- ➔ Fast asynchronous comparator
- ➔ Rail-to-rail input range
- ➔ One positive input, two negative inputs selectable by a digital pin
- ➔ Designed with IO transistors
- ➔ 9 μA dynamic current consumption
- ➔ Less than 1.3 nA current consumption in power down mode
- ➔ Portable to any CMOS logic process with 6 (or more) metal mask layers and 3.3 V transistors (or 2.5 V overdrive)
- ➔ Propagation delay of 0.2 μs

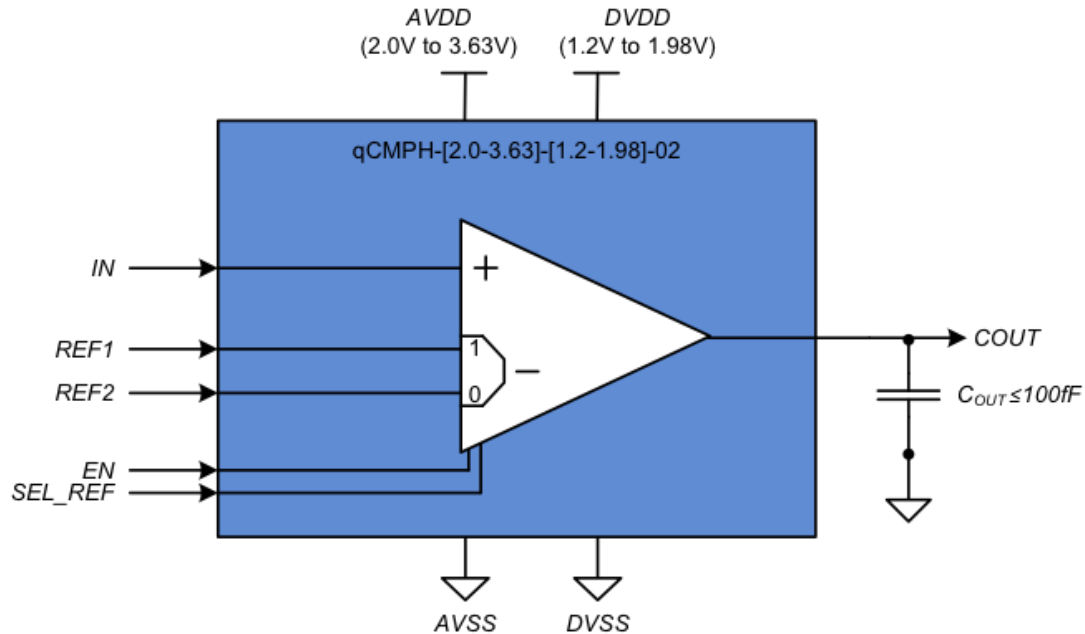
- **qCMPH-LP-[2.0-3.63]-[1.2-1.98].02**

- ➔ Low quiescent current comparator
- ➔ Rail-to-rail input range
- ➔ One positive input, two negative inputs selectable by a digital pin
- ➔ Designed with IO transistors
- ➔ 1.2 μA current consumption
- ➔ Portable to any CMOS logic process with 6 (or more) metal mask layers and 3.3 V transistors (or 2.5 V overdrive)
- ➔ Propagation delay of 2 μs

SYNOPSIS



APPLICATION SCHEMATIC



RELATED PRODUCTS

- Reusable Power Kit Library supplying diverse optimized voltage regulators and complements for power management
- Mixed signal schematic editor and simulator for the design and validation of our components
- Library of Standard cells and memories
 - ➔ optimized for high density and low power consumption
 - ➔ ultra low leakage Standard cells Libraries enabling direct battery connexion
 - ➔ enabling island partitioning
- Power optimized processor ranging from 8 bits to 32 bits
- High resolution analog converters for audio or measurement applications

DELIVERABLES

- **Front-end deliverables**
 - ➔ ViC specifications and User's manual
 - ➔ Digital Place Holder Model (DPHM) (Verilog)
 - ➔ Electrical Performance Logic and Analog Model (EPLAM) (Verilog-AMS)
 - ➔ Footprint (LEF)
 - ➔ Timing files (.lib)
- **Back-end deliverables**
 - ➔ GDS Socket (GDSII)
 - ➔ Flattened SPICE netlist for LVS purpose to the targeted foundry (SPICE)
 - ➔ GDSII database to the targeted foundry (GDSII)